CLAIMS

What is claimed is:

1. A system for connection to at least one integrated circuit device on a wafer, comprising:

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between said bottom surface and said top surface;

a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips for connection to said at least one integrated circuit device, and a plurality of electrical connections extending through said substrate between each of said plurality of said spring probe contact tips and said connector surface;

a plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board;

at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of said electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of said at least one interconnection region; and

means for fixedly holding each of said at least one interface module in relation to said system board, such that said plurality of electrically conductive pads on said planar region of each of said at least one interface module contact at least one of said plurality of electrical conductors on said top surface of said system board.

2. The system of Claim 1, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographically patterned springs.

3. The system of Claim 1, wherein said plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board are flexible spring probes on said connector surface of said substrate.

4. The system of Claim 3, wherein said flexible spring probes on said connector surface of said substrate are photolithographically patterned springs.

5. The system of Claim 1, wherein said plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board are flexible spring probes on said bottom surface of said system board.

6. The system of Claim 5, wherein said flexible spring probes on said bottom surface of said system board are photolithographically patterned springs.

7. The system of Claim 1, wherein each of said at least one interface module includes a circuit having a first surface and a second surface, and wherein said plurality of electrically conductive pads are located on said first surface.

8. The system of Claim 7, wherein said circuit is a flexible circuit.

9. The system of Claim 7, wherein said circuit is a semi-rigid circuit.

10. The system of Claim 7, wherein said circuit is a rigid circuit.

11. The system of Claim 1, further comprising:

an interposer substrate located between said connector surface of said substrate and said bottom surface of said system board, wherein said plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board are located within said interposer substrate.

12. The system of Claim 1, further comprising:

at least one buss bar electrically connected to at least one of said at least one said interconnection region.

13. The system of Claim 12, further comprising:

at least one power control module located on said at least one interface module, each of said at least one power control module electrically connected

between said at least one buss bar and at least one of said at least one said interconnection region.

14. The system of Claim 13, wherein said at least one power control module is in thermal contact with said at least one buss bar.

15. The system of Claim 12, further comprising:

at least one power control module located on said at least one buss bar, each of said at least one power control module electrically connected between said at least one buss bar and at least one of said at least one said interconnection region.

16. The system of Claim 15, wherein said at least one power control module is in thermal contact with said at least one buss bar.

17. The system of Claim 1, further comprising:

at least one lower substrate standoff fixedly attached to said probe surface of said substrate.

18. The system of Claim 1, further comprising:

a travel limit mechanism which limits perpendicular travel of said substrate in relation to said system board.

19. The system of Claim 1, wherein said substrate includes a plurality of holes defined therethrough between said probe surface and said connector surface, and wherein each of said plurality of electrical connections between each of said contact tips and each of said electrically conductive connections are electrically conductive vias located within each of said plurality of holes in said substrate.

20. The system of Claim 1, wherein said substrate is electrically insulative.

21. The system of Claim 1, wherein said substrate is dielectric.

22. The system of Claim 1, wherein said substrate is electrically conductive.

23. The system of Claim 1, wherein said substrate is comprised of a material having a similar thermal coefficient of expansion to said wafer.

24. The system of Claim 1, further comprising:
an assembled component located on said substrate.

25. The system of Claim 24, wherein said assembled component is a passive component.

26. The system of Claim 25, wherein said passive assembled component is a capacitor.

27. The system of Claim 24, wherein said assembled component is an active component.

28. The system of Claim 1, further comprising:
a component incorporated as a fabricated structure of said substrate.

29. The system of Claim 28, wherein said fabricated structure is a passive component.

30. The system of Claim 29, wherein said passive fabricated structure is a capacitor.

31. The system of Claim 28, wherein said fabricated structure is an active component.

32. The system of Claim 1, wherein said substrate comprises silicon.

33. A system for connection to at least one integrated circuit device on a wafer, comprising:

a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips for connection to said at least one integrated circuit device, and a plurality of electrical connections extending through said substrate between each of said plurality of said contact tips and said connector surface;

at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of said electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of said at least said interconnection region; and

a plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and said plurality of electrically conductive pads located on said planar region of said at least one interface module; and

means for fixedly holding each of said at least one interface module in relation to said substrate, such that said plurality of electrically conductive pads on said planar region of each of said at least one interface module contact at least one of said plurality of electrical connections on said connector surface of said substrate.

34. The system of Claim 33, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographic springs.

35. The system of Claim 33, wherein said plurality of electrical connections on said connector surface of said substrate are flexible spring probes.

36. The system of Claim 35, wherein said flexible spring probes on said connector surface of said substrate are photolithographic springs.

37. The system of Claim 33, wherein each of said at least one interface module includes a circuit having a first surface and a second surface, and wherein said plurality of electrically conductive pads are located on said first surface.

38. The system of Claim 37, wherein said circuit is a flexible circuit.

39. The system of Claim 37, wherein said circuit is a semi-rigid circuit.

40. The system of Claim 37, wherein said circuit is a rigid circuit.

41. The system of Claim 33, further comprising:

at least one buss bar electrically connected to at least one of said at least one said interconnection region.

42. The system of Claim 41, further comprising:

at least one power control module located on said at least one interface module, each of said at least one power control module electrically connected

between said at least one buss bar and at least one of said at least one said interconnection region.

43. The system of Claim 42, wherein said at least one power control module is in thermal contact with said at least one buss bar.

44. The system of Claim 41, further comprising:

at least one power control module located on said at least one buss bar, each of said at least one power control module electrically connected between said at least one buss bar and at least one of said at least one said interconnection region.

45. The system of Claim 44, wherein said at least one power control module is in thermal contact with said at least one buss bar.

46. The system of Claim 33, further comprising:

at least one lower substrate standoff fixedly attached to said probe surface of said substrate.

47. The system of Claim 33, further comprising:

a travel limit mechanism which limits perpendicular travel of said substrate in relation to said at least one of said at least one interface module.

48. The system of Claim 33, wherein said substrate includes a plurality of holes defined therethrough between said probe surface and said connector surface, and wherein each of said plurality of electrical connections between each of said contact tips and each of said electrically conductive connections are electrically conductive vias located within each of said plurality of holes in said substrate.

49. The system of Claim 33, wherein said substrate is electrically insulative.

50. The system of Claim 33, wherein said substrate is dielectric.

51. The system of Claim 33, wherein said substrate is electrically conductive.

52. The system of Claim 33, wherein said substrate is comprised of a material having a similar thermal coefficient of expansion to said wafer.

53. The system of Claim 33, further comprising:
an assembled component located on said substrate.

54. The system of Claim 53, wherein said assembled component is a passive component.

55. The system of Claim 54, wherein said passive assembled component is a capacitor.

56. The system of Claim 53, wherein said assembled component is an active component.

57. The system of Claim 33, further comprising:
a component incorporated as a fabricated structure of said substrate.

58. The system of Claim 57, wherein said fabricated structure is a passive component.

59. The system of Claim 58, wherein said passive fabricated structure is a capacitor.

60. The system of Claim 57, wherein said fabricated structure is an active component.

61. The system of Claim 33, wherein said substrate comprises silicon.

62. An interface module, comprising:
an electrically insulative module base extending from a planar region;
a plurality of electrically conductive pads located on said planar region of said electrically insulative module base;
a power control module in contact with said electrically insulative module base, and having at least one electrical connection to one of said plurality of electrically conductive pads; and
an electrical conductor in electrical contact and in thermal contact with said power control module, a portion of said electrical conductor extending from said electrically insulative module base.

63. The interface module of Claim 62, further comprising:

a plurality of conductive traces connected to said plurality of electrically conductive pads located on said planar region and extending to a link connection.

64. The interface module of Claim 62, further comprising:

at least one electronic component located on said electrically insulative module base; and

at least one component trace connected between said least one electronic component and said link region.

65. The interface module of Claim 62, further comprising:

at least one electronic component located on said electrically insulative module base; and

at least one component trace connected between said least one electronic component and at least one of said plurality of electrically conductive pads located on said planar region.

66. The interface module of Claim 62, further comprising:

at least one electronic component located on said electrically insulative module base; and

at least one component trace connected between said least one electronic component and at least one of said plurality of electrically conductive pads located on said planar region.

67. The interface module of Claim 62, further comprising:

a plurality of spring probes connected to said plurality of electrically conductive pads and extending from said planar region of said electrically insulative module base.

68. The interface module of Claim 67, wherein said plurality of spring probes are photolithographically patterned springs.

69. A process, comprising the steps of:

providing a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips, and a plurality of

electrical connections extending through said substrate between each of said plurality of said contact tips and said connector surface;

providing a wafer having a lower surface and an upper surface, and having a plurality of pads located on said upper surface;

attaching said wafer to a wafer carrier;

providing a carrier ring having a hollow portion defined therethrough;

attaching said substrate to said carrier ring, such that said substrate is generally located within said hollow portion of said carrier;

bringing said attached substrate and said attached wafer into alignment, such that said plurality of spring probe contact tips on said probe surface of said attached substrate are in alignment to said plurality of pads located on said upper surface of said wafer; and

moving said carrier ring and said wafer carrier into contact, such that said aligned plurality of spring probe contact tips on said probe surface of said attached substrate contact said aligned plurality of pads located on said upper surface of said wafer.

70. The process of Claim 69, wherein said step of attaching said wafer to said wafer carrier includes aligning said wafer to said wafer carrier.

71. The process of Claim 69, wherein said step of attaching said substrate to said carrier ring includes aligning said substrate to said carrier ring.

72. The process of Claim 69, wherein said alignment between said attached substrate and said attached wafer is an optical alignment.

73. The process of Claim 69, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographically patterned springs.

74. The process of Claim 69, wherein said plurality of electrical connections which extend to said connector surface on said substrate include flexible spring probes on said connector surface of said substrate.

75. The process of Claim 74, wherein said flexible spring probes on said connector surface of said substrate are photolithographically patterned springs.

76. The process of Claim 69, further comprising the step of:

attaching said carrier ring to said wafer carrier.

77. The process of Claim 69, further comprising the steps of:

proving a test structure having a bottom surface, and a plurality of electrical conductors located on said bottom surface;

bringing said test structure and said carrier ring into alignment, such that said plurality of electrical conductors located on said bottom surface of said test structure are in alignment to said plurality of electrical connections on said connector surface of said substrate; and

moving said aligned test structure and said carrier ring, such that said aligned plurality of electrical conductors located on said bottom surface of said test structure contact said aligned plurality of electrical connections on said connector surface of said substrate.

78. The process of Claim 77, wherein said alignment between said test structure and said carrier ring is a mechanical alignment.